Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.066”**

**GATE**

**SOURCE**

**.129”**

**Top Material: Al**

**Backside Material: V Ni Ag**

**Bond Pad Size: .012 x .012” Min.**

**Backside Potential: DRAIN**

**APPROVED BY: DK DIE SIZE .066” X .129” DATE: 9/8/21**

**MFG: INFINEON THICKNESS .007” P/N: IPC055N03L3**

**DG 10.1.2**

#### Rev B, 7/1